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09/545,182	04/07/2000	Yu-Chung C. Liao	723-840	1510

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Nixon & Vanderhye P C
1100 North Glebe Rd
8th Floor
Arlington, VA 22201-4714

EXAMINER	
PAN, DANIEL H	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/545,182	Applicant(s) LIAO ET AL.
	Examiner	Art Unit 2100

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24* is/are allowed.

6)☒ Claim(s) *1-23 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 April 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Clams 1-28 are presented for examination.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 20, 21 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6571,328. Although the conflicting claims are not identical, they are not patentably distinct from each other because :

a) although claim 20 of the present application recites "floating point instruction" (see line 4) instead of the "multiply-add instruction" as recited in patented claim 1 (see line 5), it would have been obvious to one of ordinary in the art to recognize that the multiply-add instruction was applicable as a floating point instruction giving the fact that the multiply- add combination must involve a more complex level of operations such as the floating point, and the patented claim 1 did showed the usage of a floating point field 6-10 bits, which indicated the applicability of the floating

point, and it is for this reasons, the present claim is found to be obvious from the patented claim ;

b) although the patented claim 1 has the additional feature of the secondary op code indicates the high order word to be used as scalar in compared to claim 21 of the present application, one of ordinary skill in the art should be able to recognize the omission of the secondary opcode designating the order or mode of instruction word would not have affected the main scope of the invention because the secondary opcode was encoded within the same instruction format in a given instruction entity with the primary opcode, the high or low order was directed to the position change, not the change in functionality.

3. Claim 22 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2 of U.S. Patent No. 6571,328. Although the conflicting claims are not identical, they are not patentably distinct from each other because :

a) although the patented claim 2 has the additional feature of the secondary op code indicates the low order word to be used as scalar in compared to the claim 22 of the present application, one of ordinary skill in the art should be able to recognize the omission of the secondary opcode designating the order or mode of instruction word would not have affected the main scope of the invention because the secondary opcode was encoded within the same instruction format in a given instruction entity with the primary opcode, the high or low order of the instruction word was directed to the position change, not the change in functionality.

4. Claim 25 26 and 27 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 7 of U.S. Patent No. 6571,328. Although the conflicting claims are not identical, they are not patentably distinct from each other because :

a) although claim 25 of the present application recites "floating point instruction" (see line 2) instead of the multiply-add instruction as in patented claim 7 (see lines 3-4), it would have been obvious to one of ordinary in the art to recognize that the multiply-add instruction was applicable as a floating point instruction as the multiply- add combination must involve a more complex level of operations such as the floating point, and the patented claim 7 did showed the usage of a floating point field 6-10 bits;

b) although the patented claim 7 has the additional feature of the secondary op code indicates the high order word to be used as scalar as in compared to the claim 26 of the present application, one of ordinary skill in the art should be able to recognize the omission of the secondary opcode designating the order or mode of instruction word would not have affected the main scope of the invention because the secondary opcode was encoded within the same instruction format in a given instruction entity with the primary opcode, designating the secondary opcode, such as the high or low word, was directed to the position change and would not affect the main scope and the functionality of the invention.

As to claim 27, claim 27 is the same as claim 26 exec pet it is reciting the multiply-add low instruction , instead of the multiply-add high as in claim 26. The patented claim 7 has the additional feature of the secondary op code indicates the high order word to be used as scalar in compared to the claim 27 of the present application, one of ordinary skill in the art should be able to recognize the omission of the secondary opcode designating the order or mode of instruction word would not have affected the main scope of the invention because the secondary opcode was encoded within the same instruction format in a given instruction entity with the primary opcode, designating the secondary opcode, such as the high or low word, was directed to the position change and would not affect the main scope and the functionality of the invention. As to the feature of multiply-add low instruction, the examiner holds that the high and low order of the instruction was directed to the position change , and would not affect the scope of the invention, and therefore, it is for this reasons claim 27 is found to be obvious from the patented claim 7.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3,6,7,9,11,12,14-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Hinds et al. (6,170,001).

6. As to claim 1, Hinds disclosed scalar and vector system as claimed comprising at least :

a) providing a vector [v] in a vector register file (see fig.2. [38], see registers s8-332 for storing the vector in);

b) embedding a location identifier (see the operand specifying field [s]) of the scalar value within the vector in bits (see each register has 32 bits) comprising mixed vector and scalar instruction v=v op s).

7. As to claim 2, the vector instruction was also provided in a bit form (see the 32 bit long vector register v which provided location identifier [s] (see the s operand specifier for accessing the scalar value in col.6, lines 45-60, col.7, lines 20-33).

8. As to claim 3, Hinds also had dimension of 2^n because it was a binary 32-bit in length ; the least bit should be 2^0 (2^0 = 1) and the most bit 2^5 (2^5 = 32).

9. As to claim 6, Hinds also included two single precisions [s] in a vector [v} (see fig.15, see the pairs of single precisions in col.13, lines 22-29)

10. As to claims 7,11, Hinds also included a vector register file (e.g. see fig.2 38) and an instruction set (s= S*S, v= s* v, v=v*v) including at least one mixed vector and

scalar instruction (see v= v*s) having a bit format (see the bit length) in which a location identifier (see the register specifier, see col.7, lines 21-30, see also col.6, lines 45-60 for register specifiers) in thin a vector needed to execute the instruction was embedded.

11. No distinction between the instruction and the opcode has been recited in claim 7, therefore the embedded address in the instruction is treated as any access information (see the register specifier [s]) inserted in the instruction as the operand , not in the opcode.

12. As to claim 9, the register specifier of Hinds had to have at least one dedicated bit to specify the location, otherwise, it would not work. In other words, if there were no at least a single bit, it could not have worked.

13. As to the 2^n dimension in claim 10, see discussion for claim 3.

14. As to claim 12, applicant is referring to the $2^n = 2$, when n = 1. Examiner believes this is not an inventive feature since any bit format (including the vector and scalar) of a conventional instruction format (e.g. 4,8,16, 32 etc) must include at least 2 bit-long length. In addition, there is no limitation (either connections or functionality) showing 2 bit dimension was special in the claim, therefore, the dimension of 2 is found not to be distinguishable from the prior art. Applicant is welcome to provide feedback in the next response.

15. Claim 12 is recited as to be dependent from claim 1, however, examiner believes it was meant to be dependent from claim 7 because it is referring to the data processor

(claim 7) , not the method in claim 1. For the purpose of examination, claim 12 is assumed to be dependent from claim 7. See also claim 13 for the same problem.

16. As to claims 14,18, Hinds also included bit format designating a first source vector register [v], bits designating a second source vector register [v], and bits designating location of a scalar operand within a vector for execution (e.g. see col.7, lines 16-33 for background, see the 3 operands used in instruction v= s* v + v in col.23, table 2, table 4, see specific bit implementations in tables 13-14, see also col.21, lines 1-67, col.22, lines 1-67, col.23, lines 1-67 for mixed vector and scalar operands and registers designations, see also col.27, lines 31-35 for the instruction format).

17. As to claim 15, Hinds also indicated the scalar location within a source vector (e.g. see the overlapped scalar registers and vector register in col.22, lines 25-56, col.23, lines 19-50, line 67).

18. As to claim 16, Hinds also included primary opcode and secondary opcode encoding (e.g. see the opcode field encoding in table 14).

19. As to claim 17, Hinds also included the bits (see instruction format in col.25,27,28) embedding the scalar location indicator (see the destination address operand) within a vector register (see the overlapped scalar with vector in col. 23, 24) and at least one opcode (see the 3 bit opcode, for second opcode see instruction format in col.33).

20. As to claim 19, Hinds also included paired single units (e.g. see the paired single precisions [s} in fig.15).

21. Claims 4,5, 8, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinds et al. (6,170,001) as applied to claims 1,7, above, and further in view of Pawloski (5,255,382).

22. As to claims 4,8, Hinds did not specifically teach the location identifier was embedded into the opcode as claimed., Instead , the location identifier [s] used to specify the scalar address was an operand, not the opcode. However, Pawloski disclosed a system for embedding a location identifier [target address] into an opcode (e.g. see col,5, lines 29-31). It would have been obvious to one of ordinary skill in the art to use Pawloski in Hinds for embedding the location identifier in the opcode as claimed because the use of Pawloski could provide Hinds the direct control ability to the scalar value by the opcode, thereby reducing the extra access cycle and also minimizing the circuit space, and it could be achieved by defining the location identifier (e.g. the target address) of Pawloski into the configuration file of Hinds such that the location identifier could be recognized by Hinds' opcode byte, and because Hinds also disclosed that his system need to know whether any particular data word forms a first or second type which need to be available in subsequent executed processes (e.g. see col.2, lines 2-5),

and that the more opcode bit space was made available (col.7, lines 36-41), which was a suggestion of the need of a direct control on the operand of a given type in order to reduce the latency for subsequent processes, and the possibility of inserting additional information into the opcode, and Pawloski's embedded opcode address could have provided the solution to the problem, and in doing provided a motivation.

23. As to claim 5, Hinds also taght secondary opcode (e.g. see Op[0] in col.33, the instruction format). Since Pawloski already taught the embedded address in opcode in addition to Hinds (see discussions in paragraph # 22 above), embedding the address into secondary opcode was also achievable.

24. As to claim 13, Hinds also included two single precisions (e.g. see the pairs of single precisions in col.12, lines 25-43). For examination purpose, claim 13 is assumed to be dependent from claim 8. Applicant is kindly suggested to provide feedback in the next response.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Meier et al. (6,105,129).

26. As to claim 23, Meier disclosed a system including a decoder for decoding some graphic instructions (see the multimedia instructions for video application in col.5,

lines 48-52, see also the decoder providing control information at the output in col.9, lines 22-29) and at least one paired singles instruction (see fig.5 [100F], see the two singles in col.19, lines 22-30), wherein the decoder was operable to decode special purpose register command including a bit pattern or encoding (e.g. see col.7, lines 40-50) for enabling the paired single operations (e.g. see also the decoding of the multimedia instructions to the function unit in col.13, lines 13-39). Meier did not specifically show his decoder including a special purpose register bit in the third bit position as claimed. However, since no other bit position connections being recited with the third bit, the third bit seems to be an arbitrary bit position. Therefore, any bit position can be used to enable the operation. And, it is for this reason, the particular bit position is not given a patentable weight unless that particular bit position is the only bit choice among all other bits. Therefore, it would have been obvious to one of ordinary skill in the art to use the third bit position as claimed because specific choice of bit position would not affect the enabling functionality. Applicant is welcome to provide feedback or explanation why the third bit position would make a major difference instead of the use of other bit position or other bit pattern in the next response. In summary, although Meier did not specifically show the third bit, Meier's decoder showed the control information at the output of the decoder for enabling the operation (e.g. see col.9, lines 22-29), it would have been obvious to one of ordinary skill in the art to use a third bit for control purpose because the order of the bit position would not affect the enabling function of the operation. Applicant is welcome to provide feedback in the next response.

27. Claim 24 is allowable over the art of record for reciting the combined features of the bit designations of the primary and secondary opcode, and the detailed structures of the pair of the single-scalar-vector-multiply high instruction , and the pair of the single-scalar-vector-multiply low instruction (claim 24).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Panwar (5,884,070) is citd for the background teaching of the pair of signle instructions (e.g see col.8, lines 32-39);

b) Park (6,006,315) is cited for showing the teaching of instruction bit format of vector and scalar values (e.g. see col.5, lnes 1-9, lines 41-49).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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